WHAT IS CLAIMED IS:

1. A method for processing data packets within a communication system comprising:

receiving a first data packet having a plurality of bytes of data;

determining whether the first data packet ends with an invalid byte of data;

if an invalid byte of data is detected in the first data packet, dropping the invalid byte of data;

receiving a second data packet having a plurality of bytes of data;

shifting a byte of data from the second packet in place of the dropped invalid byte of data in the first packet; and

continue shifting data one byte at a time in the second data packet.

2. The method of claim 1 wherein each byte of data in a data packet forms one half of a data word.

3. The method of claim 2 wherein each data word comprises a first 16-bit byte and a second 16-bit byte, and the communication system is a synchronous optical network (SONET).

4. A method for processing data packets within a communication system, the method comprising:

receiving a first data packet in the communication system, the first packet ending with a valid byte and an invalid byte of data;

dropping the invalid byte of data;

receiving a second data packet that begins with a first valid byte of data; and

concatenating the valid byte of the first data packet with the first valid byte of the second data packet.

5. The method of claim 4 wherein the second data packet further comprises a second valid byte, a third valid byte and a fourth invalid byte.

6. The method of claim 5 further comprising shifting the second valid byte into a location previously occupied by the first valid byte.

7. The method of claim 6 further comprising shifting the third valid byte into a location previously occupied by the second valid byte.

8. The method of claim 5 further comprising flagging the fourth invalid byte as invalid.

9. The method of claim 4 wherein the act of concatenating further comprising concatenating the valid byte of the first data packet and the valid byte of the second data packet into a 128 bit envelope.

10. The method of claim 4 wherein the second data packet is 16 bits.

11. The method of claim 4 wherein the communication system is a synchronous optical network (SONET).

12. The method of claim 4 wherein the act of concatenating further comprises linking the valid byte of the first data packet and the valid byte of the second data packet into a high speed packed.

13. The method of claim 12 wherein the high speed packet is 128 bits.

14. The method of claim 11 wherein concatenating occurs at an interface between a framing chip and a system chip.

15. A concatenation circuitry, comprising:

a first multiplexing logic circuitry having a data output port, a data select port, and first and second data input ports, the data select port for selectively coupling any one of the first, or second data input ports to the data output port;

a first register, having a data input port for receiving input data and a data output port for coupling to the first data input port of the multiplexing logic circuitry;

a second register having a data input port for receiving input data, and for coupling to the data input port of the first register, the second register having a data output port for coupling to the second data input port of the multiplexing logic circuitry;

a third register having a data input port for coupling to the data output port of the first multiplexing logic circuitry, and a data output port for outputting data;

a fourth register having a data input port, and a data output port for outputting data; and

a second multiplexing logic circuitry having a first data input port for coupling to the data output port of the second register, the second multiplexing logic circuitry having a second data input port for coupling to the input port of the second register, the second multiplexing logic circuitry having a data output port for coupling to the data input port of the fourth register, the second multiplexing logic circuitry having a data select port for selectively coupling either the first data input port or the second data input port with the data output port of the second multiplexing logic circuitry.

16. The circuitry of claim 15 wherein the data output port of the fourth register is for bits 0 through 7.

17. The circuitry of claim 15 wherein the data output ort of the third register is for bits 8 through 15.

18. A logic circuitry for processing data packets within a communication system such that data packets contain valid bytes of data, the circuitry comprising:

logic circuitry for determining that a first packet ends with a valid byte and an invalid byte of data;

logic circuitry for dropping the invalid byte of data;

logic circuitry for determining that a second data packet that begins with a valid byte of data; and

logic circuitry for concatenating the valid byte of the first data packet with the valid byte of the second data packet.

19. The logic circuitry of claim 18 further comprising logic circuitry for linking the valid byte of the first data packet and the valid byte of the second data packet into a high speed packed.

20. The logic circuitry of claim 18 wherein the high speed packet is 128 bits.

21. The logic circuitry of claim 18 wherein the first data packet is 16 bits wide.

22. The logic circuitry of claim 18 wherein concatenating occurs at an interface between a framing chip and a system chip.

23. A circuit for processing packets of data wherein a packet includes one or more words each having a first byte and a second byte, the circuit comprising:

a first register coupled to receive and store the first byte of each word;

a second register coupled to receive and store the second byte of each word;

a third register coupled to the first register and configured to receive and store contents of the first register in response to a clock signal;

a fourth register coupled to the second register and configured to receive and store contents of the second register in response to the clock signal; and

a multiplexing circuit coupled to the third and fourth registers and configured to selectively rearrange pairing of bytes.

24. The circuit of claim 23 wherein the multiplexing circuit comprises a first multiplexer having a first input coupled to an output of the third register, and having a second input coupled to an output of the fourth register.

25. The circuit of claim 24 wherein the multiplexing circuit comprises a second multiplexer having a first input coupled to an output of the fourth register, and having a second input coupled to an input of the third register.

26. The circuit of claim 25 further comprising control logic circuitry coupled to a select port of the first multiplexer and a select port of the second multiplexer.